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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/881,226 | 06/12/2001 | Roger May | 015114-053300US | 7601 |

26059 7590 03/09/2004

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| EXAMINER | |
|---|---|
| SHAH, SAUMIL R | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2186 | 4 |

DATE MAILED: 03/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/881,226 | Applicant(s) MAY ET AL. | |
|---|---|---|---|
| | Examiner Saumil Shah | Art Unit 2186 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 June 2001*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-45* are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

***Election/Restrictions***

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-12, drawn to a programmable logic circuit comprising a programmable logic portion and an embedded processor portion comprising a processor and a memory block with two ports and an arbiter, classified in class 711, subclass 103.

II. Claims 13-21, drawn to a method of arbitration comprising sending lock requests and grants depending on the status of the memory ports, classified in class 711, subclass 152.

III. Claims 22-27, drawn to a method of laying out a programmable logic device, classified in class 716, subclass 8.

IV. Claims 28-31, drawn to a programmable logic circuit comprising an embedded processor portion further comprising a processor, a memory with two ports, two buses and a multiplexer, classified in class 711, subclass 103.

V. Claims 32-37 and 42-43, drawn to a programmable logic circuit comprising an embedded processor portion further comprising a processor, a memory with two ports, two buses, an arbiter, a multiplexer and a lock register to store a user-defined variable lock size, classified in class 711, subclass 103.

VI. Claims 38-41, drawn to a programmable logic circuit comprising a programmable logic portion and an embedded processor portion further

comprising a processor and a memory with two ports that have a configurable width and a configurable depth, classified in class 711, subclass 103.

VII. Claims 44-45, drawn to a programmable logic circuit comprising a programmable logic portion and an embedded processor portion further comprising a processor and two memories each having two ports which have a configurable width and a configurable depth, classified in class 711, subclass 103.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention II has separate utility such as using a lock request and grant system for the memory. Invention II also uses a lock register to store a value. For example, invention I may be used without a locking system to arbitrate between the ports.

See MPEP § 806.05(d).

3. Inventions I and III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention III has separate utility such as stretching one side of the logic device and the embedded processor. For example, invention I may have as few as three sides for the processor without any stretching.

See MPEP § 806.05(d).

4. Inventions I and IV are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention IV has separate utility such as having multiple buses coupled to the components. Invention IV has one bus coupled to the processor and another bus coupled to the memory. It also has a multiplexer with the inputs coupled to the buses. Invention I may have a common bus for all the components.

See MPEP § 806.05(d).

5. Inventions I and V are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention V has separate utility such as having separate lockable portions and unlockable portions in the memory. The arbiter determines access grants depending on the portion of memory accessed by a port. Invention V also uses a lock register to store a value. Invention I may be used without a locking system to arbitrate between the ports. Also, it may not have separate portions in the memory that are lockable.

See MPEP § 806.05(d).

6. Inventions I and VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention VI has separate utility such as memory ports with configurable width and depth. Invention I may have fixed port width and depth.

See MPEP § 806.05(d).

7. Inventions I and VII are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention VII has separate utility such as having two memories each having two ports with related widths and depths. For example, invention I may have unrelated port width and depth and only one memory.

See MPEP § 806.05(d).

8. Inventions II and III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention III has separate utility such as stretching one side of the logic device and the embedded processor. For example, invention II may have as few as three sides for the processor without any stretching.

See MPEP § 806.05(d).

9. Inventions II and IV are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention II has separate utility such

as using a lock request and grant system for the memory. Invention II also uses a lock register to store a value. For example, invention IV may be used without a locking system to arbitrate between the ports.

See MPEP § 806.05(d).

10. Inventions II and V are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention V has separate utility such as having separate lockable portions and unlockable portions in the memory. The arbiter determines access grants depending on the portion of memory accessed by a port. For example, a port in invention V does not require access grant to access a non-lockable portion even though another port may be accessing it. But a port in invention II always requires an access grant each time a port wants to access the memory.

See MPEP § 806.05(d).

11. Inventions II and VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention VI has separate utility such as memory ports with configurable width and depth. Invention II may have fixed port width and depth.

See MPEP § 806.05(d).

12. Inventions II and VII are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable In the instant case, invention VII has separate utility such

as having two memories each having two ports with related widths and depths. For example, invention II may have unrelated port width and depth.

See MPEP § 806.05(d).

13. Inventions III and IV are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention III has separate utility such as stretching one side of the logic device and the embedded processor. For example, invention IV may have as few as three sides for the processor without any stretching.

See MPEP § 806.05(d).

14. Inventions III and V are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention III has separate utility such as stretching one side of the logic device and the embedded processor. For example, invention V may have as few as three sides for the processor without any stretching.

See MPEP § 806.05(d).

15. Inventions III and VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention III has separate utility such as stretching one side of the logic device and the embedded processor. For example, invention VI may have as few as three sides for the processor without any stretching.

See MPEP § 806.05(d).

16. Inventions III and VII are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention III has separate utility such as stretching one side of the logic device and the embedded processor. For example, invention VII may have as few as three sides for the processor without any stretching.

See MPEP § 806.05(d).

17. Inventions IV and V are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention V has separate utility such as having separate lockable portions and unlockable portions in the memory. The arbiter determines access grants depending on the portion of memory accessed by a port. For example, invention IV may be used without a locking system for arbitration. Also, invention IV may not have separate lockable portions in the memory.

See MPEP § 806.05(d).

18. Inventions IV and VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention VI has separate utility such as memory ports with configurable width and depth. For example, invention IV may have fixed port width and depth.

See MPEP § 806.05(d).

19. Inventions IV and VII are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention VII has separate utility such as having two memories each having two ports with related widths and depths. For example, invention IV may have unrelated port width and depth and only one memory.

See MPEP § 806.05(d).

20. Inventions V and VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention VI has separate utility such as memory ports with configurable width and depth but no locking arbitration system. Invention V may have fixed port width and depth.

See MPEP § 806.05(d).

21. Inventions V and VII are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention VII has separate utility such as having two memories each having two ports with related widths and depths. Invention V may have unrelated port width and depth and only one memory.

See MPEP § 806.05(d).

22. Inventions VI and VII are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention VII has separate

utility such as having two memories each having two ports with related widths and depths. Invention VII also has a multiplexing circuit coupled to the second and fourth ports. For example, invention VI has only one memory and none of the ports are coupled through a multiplexing circuit.

See MPEP § 806.05(d).

23. Because these inventions are distinct for the reasons given above and the search required for any of the groups is not required for any other group, restriction for examination purposes as indicated is proper.

24. Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

25. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saumil Shah whose telephone number is 703-305-8786. The examiner can normally be reached on 9:00 AM to 5:30 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 703-305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Saumil Shah
Patent Examiner
AU: 2186

February 26, 2004

BEHZAD JAMES PEIKARI
PRIMARY EXAMINER